Learning Goals for Computer Organization II

Main theme	***Prerequisites***	***Approaching Learning Goals***	***Reaches Learning Goals***	***Deepens Learning Goals***
Digital logic	• Knows the concepts Boolean variable and truth value (Discrete mathematics)	• Can explain Boolean algebra operations, truth tables, assumptions and identities • Knows the basic gates and can explain the basic ideas and ways to describe combination and sequential circuits • Can explain the implementation of selection and (de)coding circuits • Can explain the basic idea of storing data with circuits	• Can us a functionally complete set of gates to implement gates missing from it • Can implement a given logical function with combinational circuits and optimize it with Karnaugh maps • Can explain roughly the combinatorial circuit implementation of addition and ROM-memory circuits • Can explain the operation and differences of various clocked flip-flops, as well as the implementation of registers, shift registers, and counters with flip-flops	• Can explain the Quine-McKluskey or Lugue methods to simplify combinational circuits • Can explain precisely the combinatorial circuit implementation of addition and ROM-memory circuits • Can consider timing and voltage problems in implementing circuits

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Bus operation	• Can explain the need and operation of bus hierarchy (CO-I) • Can explain how CPU operates to execute instructions (CO-I) • Knows the huge speed differences for various memory devices (CO-I)	• Can explain the usage of various buses in the system • Can explain the basic features of time-interleaved bus • can explain different bus timing schemes and data transfer types	• Knows differences of various arbitration methods and their signal level implementation • Can explain at the signal and bus event level operation for at least one bus type	• Can explain the signal level operation of the latest bus types

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Memory hierarchy	• Can explain the huge speed differences of various memory devices, as well the significance of them (CO-I) • Can explain why cache memory if needed (CO-I) • Know the basic ideas of cache and virtual memory operations (CO-I)	• Can explain the effect of temporal and spatial locality at various memory hierarchy levels • Can explain the memory implementation at combination circuit level • Can explain types and policies for various cache organization methods • Can explain the operation of paged and segmented virtual memory • Can explain inversed and multi-level virtual memory address translation concepts • Can explain the requirements and basic features for TLB operation	• Can explain he details for set-associative cache operation • Can explain the need for using hierarchical cache memories with separate instruction and data caches • Can explain the similarities and differences of TLB and cache • Can explain the precise CPU operation as related to TLB and cache loops • Can explain various replacement policies for cache memories • Can estimate the memory reference time considering both virtual memory and cache effects	• Can explain differences between Rambus DRAM and normal DRAM • Can explain TLB and cache memory details for some certain CPUs • Can explain various replacement policies for virtual memory back-up store

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Arithmetic	• Can explain addition and multiplication algorithms with paper and pencil (CO-I) • Can explain the IEEE floating point presentation (CO-I)	• Can explain integer basic arithmetic circuit level implementation • Can explain IEEE floating point presentation for very large and very small numbers • Can explain various methods for floating point rounding	• Can explain the implementation of 2's complement addition and subtraction • Can explain Booth's algorithm for multiplication • Can explain the basics of IEEE floating point arithmetic implementation	• Can explain precisely integer division implementation • Can explain detailed implementation for IEEE arithmetic implementation
Instruction sets	• Can explain how instruction execution cycle works and the differences between machine language and symbolic assembly language (CO-I) • Can explain different data reference methods as well as different data locations (CO-I)	• Can explain machine instruction components • Can explain the meaning of registers • Can explain various ways to store multi-byte data • Can compare instruction sets based on their fundamental features	• Can classify instruction sets based on their features • Can classify processors based on their instruction sets • Can explain the structure and data reference methods for real processor instruction sets	• Can give examples of Load-Store processors • Can explain registers, data types and data reference methods for Intel Pentium and IBM PowerPC processors

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Processor structure and operation	• Can explain the basic idea of von Neumann processor architecture (CO-I) • Can explain instruction fetch execute cycle operation (CO-I)	• Can explain processor general structure at register and control unit level • Can explain the basic idea of pipelining • Can explained give examples on pipeline dependency problems • Can explain the basic idea of RISC architecture, and its differences, advantages, and disadvantages as compared to CISC architecture • Can explain the basic ideas of superscalar processor and give examples of new dependency problems it causes • Can explain the basic idea of predicated execution	• Can compute the speed advantage obtained with pipelining • Can give solutions to problems caused by pipeline dependencies • Can explain register window usage to speed up procedure calls • Can explain register allocation problem solution with net-coloring problem • Can explain how RISC and CISC architectures can be combined • Can give solutions to problems caused by write- and anti-dependencies • Can explain the ideas and operations of control speculation, and software pipelining	• Can introduce special registers in Intel Pentium and IBM PowerPC and how they are used • Can explain interrupt mechanisms for Intel Pentium and IBM PowerPC • Can explain basic ideas of combining multiple processor architectures in Intel Pentium II and Transmeta Crusoe processors • Can explain exact operation in executing multiple instructions simultaneously in IBM PowerPC and Intel IA-64 processors

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Control		• Can explain how control signals for instruction fetch-execute cycle are produces with a state automata • Can explain the basic idea of micro-programmed control • Can explain the function of control memory in micro-programmed control	• Can explain the operation of hard-wired and micro-programmed control • Can explain how clock cycle length is determined • Can explain the differences, advantages and disadvantages of horizontal and vertical micro-programming • Can explain the advantages and disadvantages of various ways to select next micro-program instruction	• Can explain, how modern processor combines micro-programmed and direct control • Can explain precise implementation of some current processors