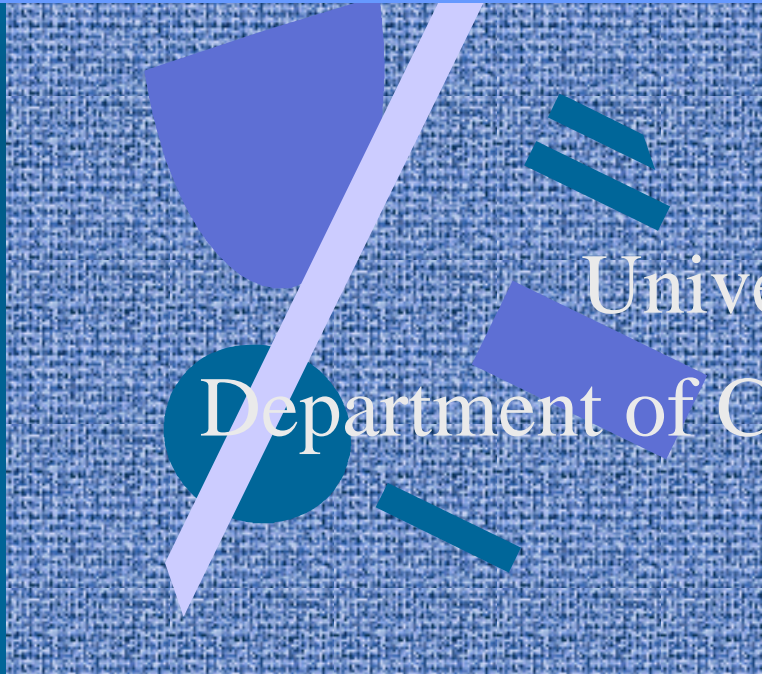


581365-8

# Computer Organization II (Tietokoneen rakenne)



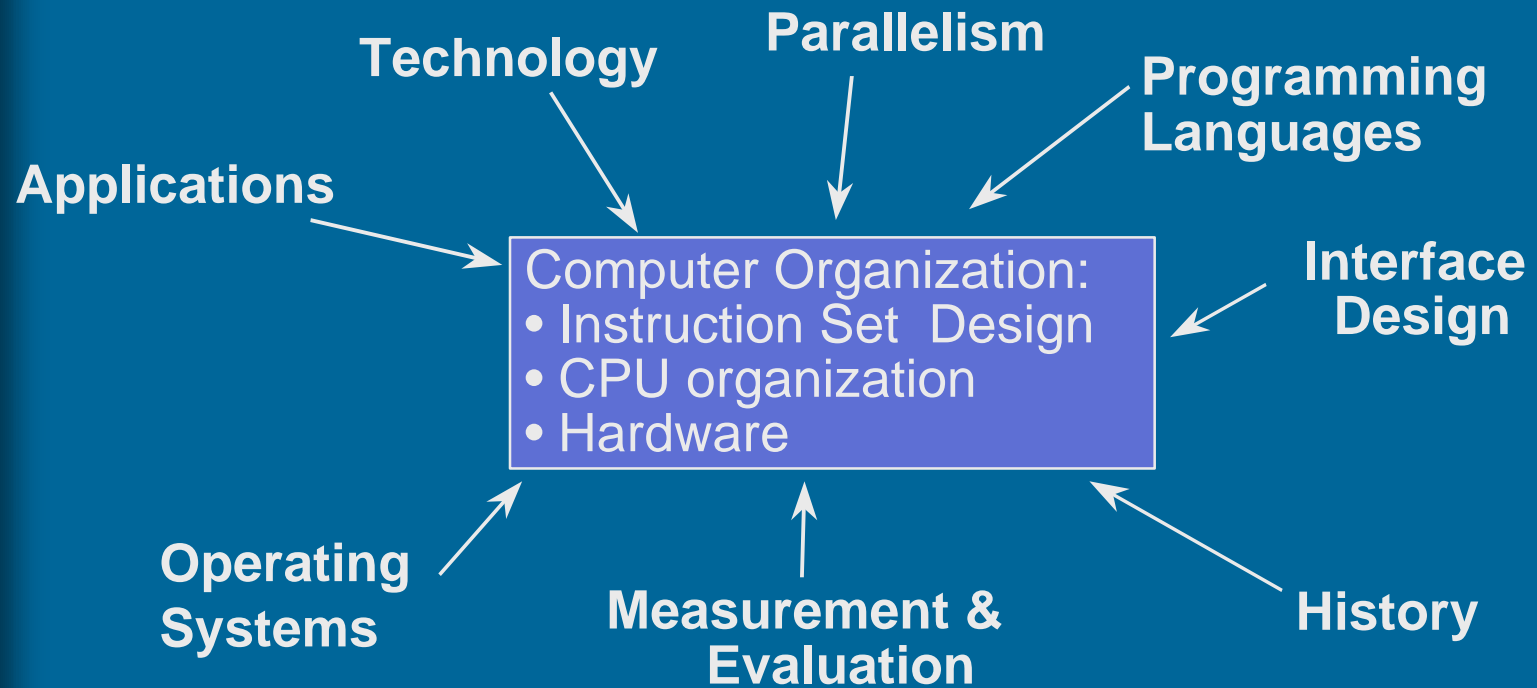
Teemu Kerola  
University of Helsinki  
Department of Computer Science

Fall 1999

# Course Focus

- Understand basic computer system design from the user (human, OS, compiler) viewpoint as well as from the designer viewpoint.
- Understand how a simple hardware clock signal makes a computer to execute programs.

# Peripheral topics



# Related Courses

**Comp. Org. I  
(TiTo)**

**Comp. Org. II  
(TiKRa)**

**Computer  
Architectures**

**Conc. Systems (Rio)  
Data Struct. (TiRa)  
Compilers (OKK)  
Oper. Systems (KJP)  
Data Comm. (TiLi)**

...

# Notice

- These slides are made to support lectures and to be used with the text book.
- They do NOT include everything that is covered in the lectures.
- They are NOT a replacement for a text book.
- If you need a self-contained presentation, please use the text book.

# Motto

- “It is not good exercise,  
if you do not sweat”

(“Kunto ei nouse, jos ei tule hiki”)



# WWW Information

- Course home page  
*<http://www.cs.helsinki.fi/~kerola/tikra/>*
- This semester schedule  
*<.../tikra/S99/aikataulu.html>*
- Lectures  
*<.../luennot/>*
- Homeworks  
*<.../laskuharj/>*
- Old exams  
*<.../tikra/kokeet/>*
- Newsgroup  
*<hy.opiskelu.tktl.tikra>*

**Comp. Org. I  
(TiTo,  
Tietokoneen  
toiminta)**

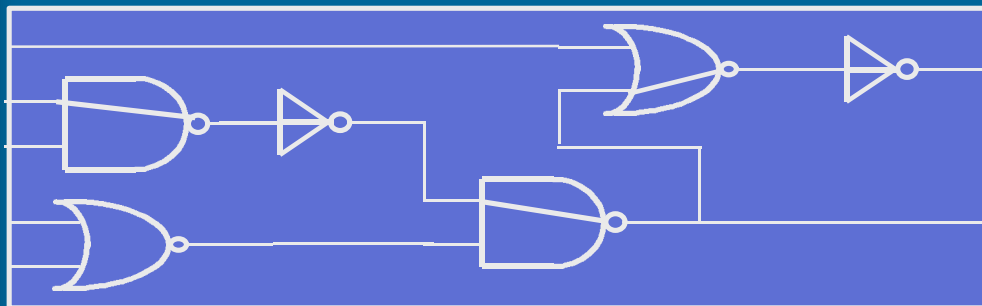
A := B + C;

High level language



```
MOV AX, B
ADD AX, C
MOV A, AX
```

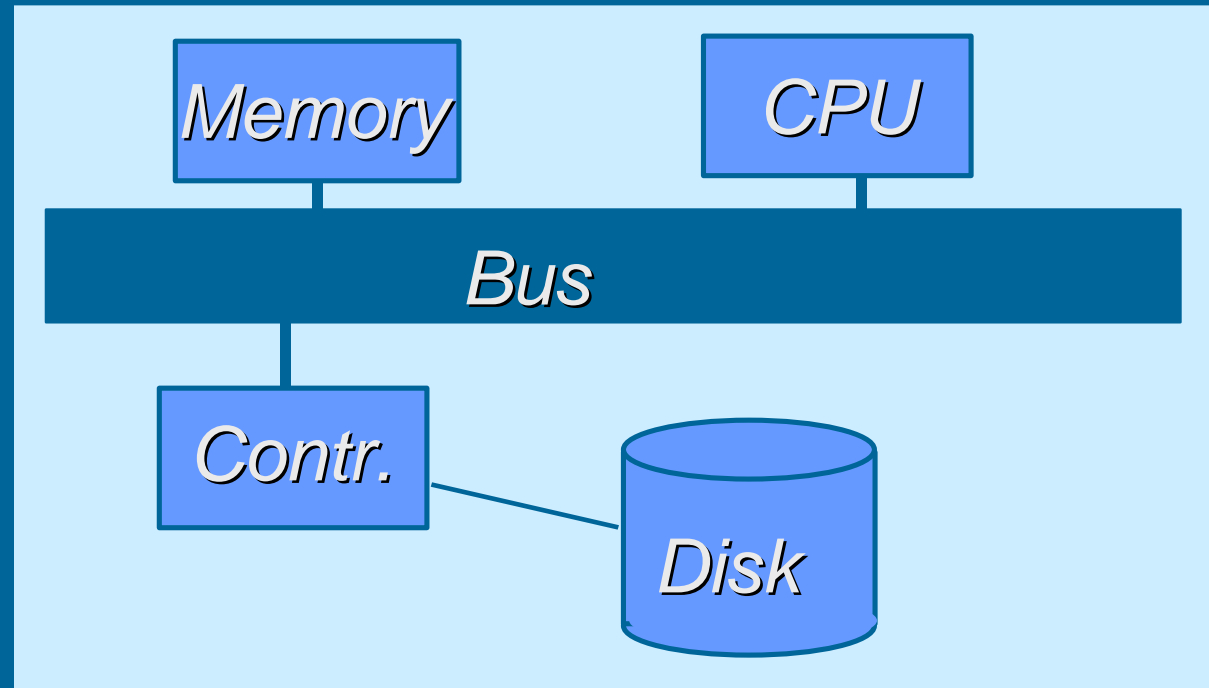
Assembler



Logic circuits

**Comp. Org. II  
(TiKRä,  
Tietokoneen  
rakenne)**

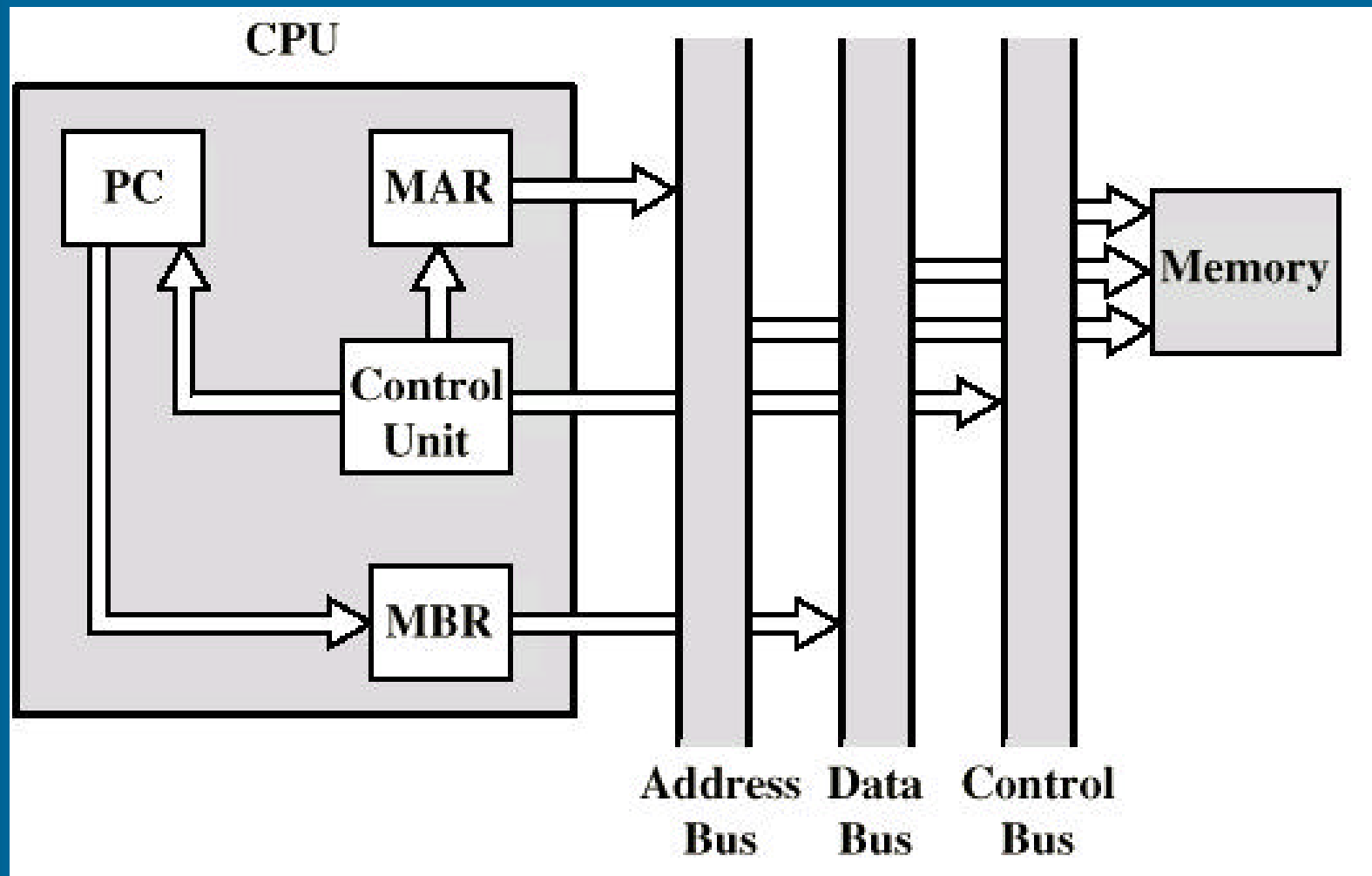




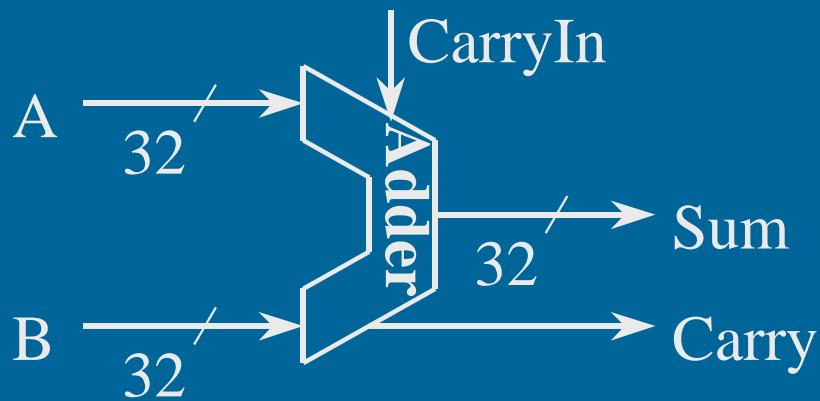
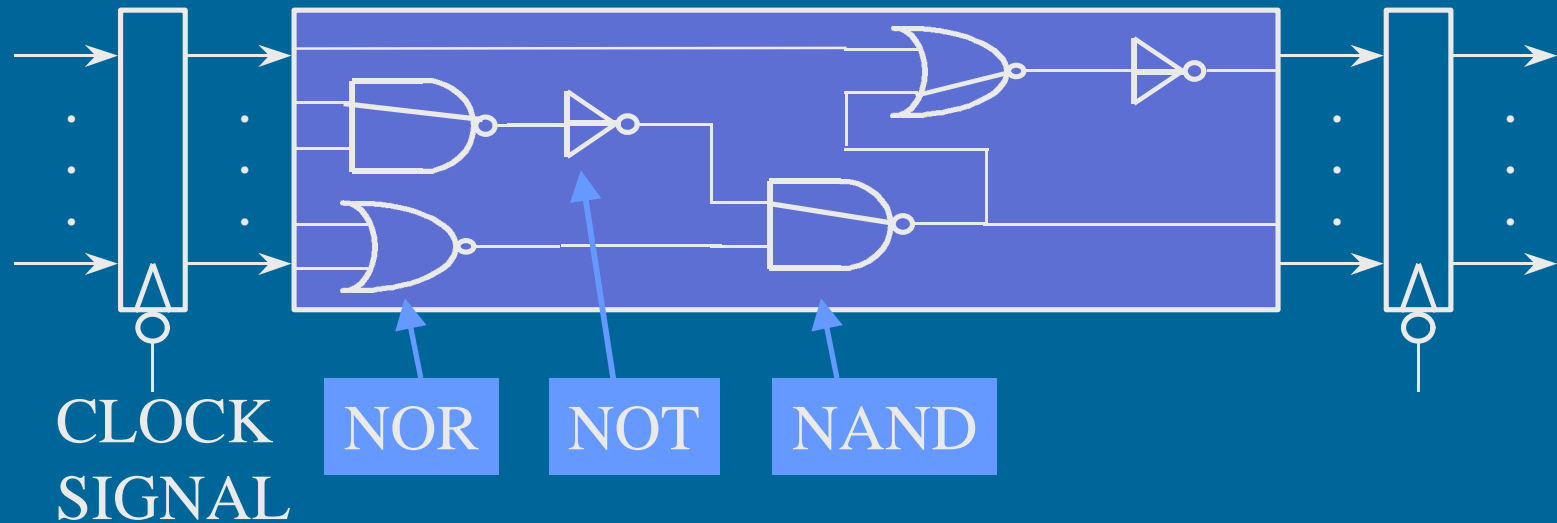
**TiTo:** What happens in system

**TiKRa:** How are CPU & memory implemented?

# The Lowest Presentation Level for Comp Org I (TiTo)



# The Lowest Presentation Level for Comp Org II (TiKRa)



# Contents

- Computer system - overall structure (Ch 1-7)
- System buses (Ch 3)
- Digital logic (App A)
- Memory hierarchy (Ch 4.3, 7.4)
- Computer arithmetic (Ch 8)
- Instruction sets (Ch 9-10)
- CPU structure and function (Ch 11)
- Reduced Instruction Set Computers (Ch 12)
- Instr. level parall. and superscalar proc. (Ch 13)
- Control unit (Ch 14-15)