

RISC Architecture

Ch 13

Some History
 Instruction Usage
 Characteristics
 Large Register Files
 Register Allocation
 Optimization
 RISC vs. CISC

Major Inventions in Computer Architecture: General purpose computer



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- Howard Aiken, Mark I, 1944
 - relays, 17m long, 2.4m tall
 - 500 miles of wire, 5 tons
 - 3 million connections
 - 6 sec mult, 12 sec div
 - IBM ASCC (automatic sequence controlled calculator)
 - turned off last time 1959



ENIAC



- J. P. Eckert and John Mauchly, 1946
 - 1500 relays
 - 18000 vacuum tubes
 - 70,000 resistors
 - 20 accumulators
 - 10 digits
 - modify program by rewiring

Stored Program Computer

- Store both program and data in memory
- John von Neumann, 1945
 - Electronic Discrete Variable Automatic Computer (EDVAC) prototype
- Maurice Wilkes, 1949
 - Electronic Delay Storage Automatic Calculator (EDSAC)
 - first fully operational stored program computer
- Software was born



Floating Point hardware



- Gene Amdahl, 1953
- IBM 704
 - OS allowed for batch processing
 - combine existing commands into new commands
 - 5 kFLOPS
 - 19 units produced

Family of computers

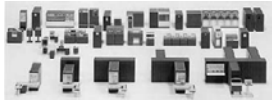
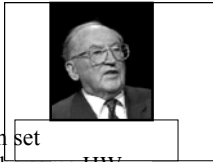
- Family of computers with different implementations of the same architecture
 - Computer system can grow within the family and all SW will still run
 - Need faster/bigger
 - ⇒ buy a faster/bigger system in the family
 - Gene Amdahl
 - IBM S/360
 - DEC PDP-8

1964



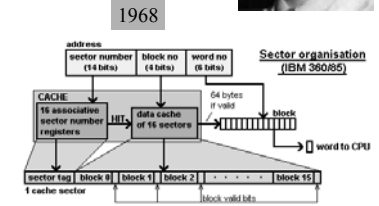
Microprogrammed control unit

- Can modify instruction set architecture (ISA) easily
- Makes it easier to implement families of systems
- Can have different instruction set architecture (ISA) on top of the same HW
- Maurice Wilkes, 1951
- IBM System/360, 1964



Cache memory

- Maurice Wilkes, 1965
- major speed up (12x ?)
- IBM System/360 Model 85



Virtual memory



- Tom Kilburn, 1962
- Atlas, 1962
 - 20 bits for virtual address space
 - 512 word (each 48 bits) page
 - 16 KB main mem
 - 2 units sold

Atlas accumulator cabinet

Pipelining

- Tom Kilburn (?)
- Atlas, 1962
 - 2 ALU's
 - overlap execution of 3 instructions



Atlas Main and B-Arithmetic Units

Multiple processors

- J. P. Eckert and John Mauchly
- Sperry Rand Univac 1108II (1108A), 1964
 - 3 CPU's
 - 2 I/O controllers
 - DMA
 - 36 bit words
 - test-and-set instruction was added for synchronization between processors



Mauchly & Univac console

RAM

- Static RAM
 - Fairchild 4100, 1970
 - 256 bits
- Dynamic Random Access Memory
 - Robert Dennard, IBM, 1966
 - Intel 1103, 1970
 - John Reed
 - 1024 bits
 - replaces magnetic core memory by 1972



Dennard



Reed

Single chip Microprocessor

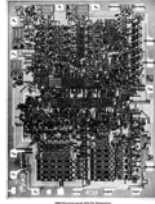
- Hoff, Faggin, Mazor
- Intel 4004, 1971
 - 2300 transistors, 60K OPS
 - "single chip which implements and interprets all microinstructions"
 - 4 bit words, 16 GPRs, 4-bit accumulator, operation register, instruction decoder
 - good for BCD operations (BCD = Binary Coded Decimal)
 - Japanese Busicom abandoned failed (!) project and bankrupted next year
 - Used in Pioneer 10 spacecraft, 1972



Faggin



Mazor



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Vector processors

- Operate on entire vectors with one instruction
- Texas Instrument Advanced Scientific Computer (ASC), 1971
 - W. Joe Watson
 - 4 pipelines
 - vectors stored in memory
 - 7 machines built
 - vectorizing Fortran compiler
 - theoretical max speed 50 MFLOPS
 - slow scalar unit



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RISC (2)

- Reduced Instruction Set Computer (RISC)
 - John Cocke, 1974
 - IBM 801 (prototype), 1974
 - project cancelled because instruction set not compatible with OS/360
- Try again ... and succeed
 - Hennessy (1981) & Patterson (1980)
 - Proved, that even CISC machines may work faster if only simple instructions and addressing modes are used



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Superscalar Processor

- ACS-1, J. Cocke, IBM Advanced Computer Systems, 1965
 - cancelled as not S/360 compatible
- Complete more than one instruction per cycle
- Targeted to normal, scalar instructions to speed up scalar processing (as opposed to vector processing)
- IBM 801 (proto design 1974), RS/6000 (1989)
- Intel i960CA (1989), Pentium (1993)
- MIPS 10000 (1995)

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Simultaneous Multithreading (SMT)

- One physical processor implements many logical processors
 - CDC 6600 I/O processor, J. Thornton, CDC, 1970
 - Susan Eggers & Hank Levy, U of Washington, 1995
- Operating systems sees many processors
- One CPU, separate register set for each logical processor
- Use memory wait stages (E.g., cache miss latencies) to run other threads (processes)
- Compaq Alpha EV-8, 4 SMT's (design 1999, dead 2001)
 - work continues at Intel for Itanium-II (2004?)
- Hyperthreads, Intel, 2001
 - Pentium 4 HT, new desktops at CS dept, late 2003 (2 hyperthreads with some 30% speedup)

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Fast Cross-platform Emulation

- Cross-platform emulation could be made faster/use less energy than direct execution
 - Edmund J. Kelly, Malcolm John Wing & Robert Cmelik, Transmeta Corp., 1996
 - Can optimize and dynamically rebuild code (translation & code optimization)
 - lots of work, possibly big gains
 - E.g., emulators for other architectures (x86)
 - do (part of) pipeline optimization by (JIT) compiler, not dynamically by complex & large HW
 - Crusoe processor, 2000

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