Name	Signature	Student Id	*Points*

Computer Organization II, miniexam 1, 28.3.2018 (13 p)

Write your answer on this exam paper in the space given. Please notice, that the exam paper is 2-sided.

a) [4 p] CPU wants to write one cache line (4 words, i.e., 16 bytes) to memory address 0x00045678. the data bus has 32 lines (+ Hamming code lines). How do you implement this with synchronic bus? Draw the timing diagram and explain what happens there.
Possible lines in your diagram are {Status lines, Address lines, Data lines, Read, Write, Acknowledge}.
Remember to mention, which component (CPU, memory) will set each new value to each line.

b) [3 p] QPI (QuickPath Interconnect) implementation has four layers: Physical, Link, Routing, Protocol. Explain for each layer, which problem they solve and how.

Why would QPI be better than bus solution? Give at least two reasons with explanations.

c) [6 p] Virtual and main memory addresses have 32 bits. Page size is 4 KB, and byte addresses are used. Set-associative TLB has 128 entries with 16 sets and set size 8. Each TLB-entry has a tag-field, 20-bit frame number, process id PID, and at least flags V (valid entry), D (dirty), R (referenced), and WP (write protect).

How do you split the 20-bit page number to fields *tag* and *set*?
Please notice, that there is no field *offset*, because each TLB "line" has only one address translation entry.

Consider a reference to virtual address 0x00045678. What are the values of fields tag and set?

Where (which entry number) in the TLB can the TLB-entry for virtual byte address 0x00045678 be located?

How is the address translation done, when there is a TLB-hit and virtual address 0x00045678 maps to physical address 0x0AACC678?

What happens in address translation, if there is a TLB-miss for virtual address 0x00045678, but no page fault?