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Computer Organization II, miniexam 2, 18.4.2018 (13 p)

Write your answer on this exam paper in the space given. Please notice, that the exam paper is 2-sided.

a) [3 p] How is (IEEE) floating point addition (X+Y) done in practice? What special cases must you consider?

What are the guard-bits and how do they relate to floating point addition?

b) [3 p] 16-bit ROM circuit has four 4-bit memory locations. Memory location 0 has value 13, location 1 has value 7, location 2 has value 8, and location 3 has value 5.

The truth table for the ROM circuit above has two inputs (A1, A2) and for outputs (V1, V2, V3, V4):

INPUT		OUTPUT				COMMENT
A1	A2	V1	V2	V3	V4	
0	0	1	1	0	1	= 13
0	1	0	1	1	1	= 7
1	0	1	0	0	0	= 8
1	1	0	1	0	1	= 5

i. [2 p] Give the implementation for the ROM circuit above, with a decoder (2 inputs, 4 outputs) and four OR gates. (When the decoder is given the address with two inputs, the corresponding output line has value 1, and other 3output lines have value 0.)

ii. [1 p] How do Karnaugh maps relate to the implementation of this combination circuit, and how could one use Karnaugh maps in principle when implementing this ROM circuit.

KÄÄNNÄ

c) [3 p] Explain the concept “RAW data hazard”, relating to pipeline implementation. What problem does a RAW data hazard cause? Give two solution methods to RAW data hazard problem, and explain briefly how they work.

d) [4 p] What pipeline problem is solved with dynamic branch prediction?
Explain in main principles, how (some) such solution method works and what do you gain with it.
As an example, use machine instruction “bzer R1, loop” in memory address 0x12345678.