Name	Signature	Student Id	*Points*

Computer Organization II, miniexam 3, 2.5.2018 (13 p)

Write your answer on this exam paper in the space given. Please notice, that the exam paper is 2-sided.

a) [3 p] Superscalar architecture *out-of-order issue with out-of-order completion* issue policy.
What does this mean in practice?

Where do you solve different types (RAW, WAR, WAW) of data dependencies?

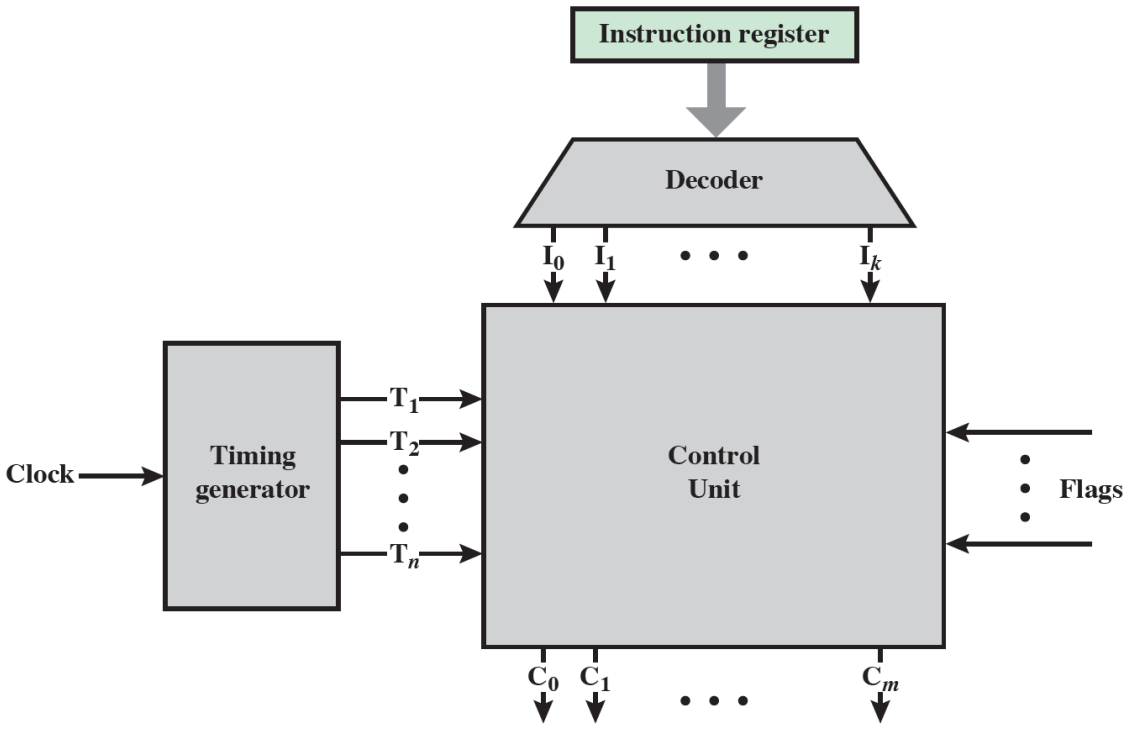
Where in the pipeline(s) an instruction will never need to wait?

b) [3 p] What is WAR dependency (hazard)? Give an instruction level example, and explain why it may slow down execution in superscalar architecture.

The effect of WAR dependency may be removed with renaming in superscalar architecture.
What does this really mean? With your example, show how WAR dependency may be removed with renaming and execution may now be faster.

TURN

c) [7 p] Hardwired control. See the picture below.



Consider implementing hardwired control according to the picture above.
What is the meaning of different signals (T_i, I_i, $Flags_i$, C_i)? How do you determine the value of (e.g.) C_3?

Assume that we are executing machine instruction ”ADD X” (add variable X value to accumulator register A), and that variable X value is already loaded to MBR.
How do you get the control signals for the micro-operations to (i) first copy MBR and AC values to ALU, (ii) then ask ALU to do the add-operation, and (iii) finally store the result in AC.

How do you move from one micro-operation to the next one?