Operating Systems, miniexam 5, 16.3.2015 (6p)

Write your answer on this exam paper in the space given. Please notice, that the <u>exam paper is 2-sided</u>.

Consider 1-level paging virtual memory with page size 4 KB. The machine instruction in execution (LOAD R4, X) is reading variable X (virtual address 0x00AABBCC) value to register R4. The system has 1-level cache.

What happens in the system when this memory reference is done in the following special cases (a and b)? Mention especially how the address translation is done. Explain also, when and how data is obtained from TLB, cache, main memory or disk. Specify the missing numerical values relating to this problem.

a) [1 p] TLB hit and cache hit?

b) [2 p] TLB miss, cache miss, and page fault?

Virtual memory page replacement algorithms

c) [1 p] How does the OPT page replacement algorithm work and what is it used for?

d) [2 p] How does the CLOCK page replacement algorithm work and what is it used for?