Computer Organization I, exam   21.12.2016

This is the course exam for lecture course. Answer all questions if you have not taken the miniexams.
Question 4 is also miniexam 4. If you already took miniexams 1-3, you need to answer only this question.
Questions 1-3 are also make-up exams for miniexams 1-3.

Please write the answer for each problem on its **own sheet** and return it in **its own pile**!
It is sufficient to give 1-2 page answer to each question.
Write on **each** answer sheat your name and signature, student id number, and course name.

1. [10 p] System structure, CPU, bus
   a. [2 p] At what parts of the instruction (fetch-execute) cycle can a memory reference occur? Explain.
   b. [2 p] At what parts of the instruction cycle can the PC value change? Explain.
   c. [2 p] How do interrupts considered in the instruction cycle?
   d. [2 p] How is supervisor (privileged) execution state considered in the instruction cycle?
   e. [2 p] How do you map a memory address used in the program (e.g., variable or instruction address 44) to (physical) main memory address (e.g., 23456)? Who makes the mapping and when?

2. [10 p] Data representation and correctness, memory
   a. [2 p] Which integer value has 16-bit two's complement little-endian representation 0xFCFD?
   b. [2 p] What is the hidden bit in the IEEE floating point standard, and what are its advantages?
   c. [2 p] How do you store string "this is a short string" in memory, to address 320?
   d. [4 p] What problem is solved with Hamming code, when would it be useful to use it, and how does work in principle?

3. [10 p] Operating systems, external memory, I/O
   a. [2 p] When do you move a process in execution state to ready-to-run state? What happens then at process management level? Give an example.
   b. [2 p] How do you move in practice, at machine language level, a process in execution state to blocked state? How is the move done? Who does the move and when? What happens next? Give an example.
   c. [2 p] How does the device driver tell a DMA device controller, what to do next?
   d. [2 p] How does the DMA device controller tell the device driver, what it has done?
   e. [2 p] Why do you usually use DMA I/O with hard disks, and not interrupt-driven I/O?

4. [10 p] Compilation, linking, loading, interpretation, emulation
   a. [2 p] How are the symbol table values for symbols X and ELSE determined in the symbolic machine language assembly, when X is a variable, and ELSE is the instruction address of else branch used in conditional branching.
   b. [2 p] What problem is solved with linking? As an example, use service function CURR_TIME in module TIMERS.
   c. [3 p] How does computation in Java Virtual Machine (JVM) differ from that in ttk-91? How do the registers and their use in JVM differ from that in ttk-91?
   d. [3 p] P is a program written in Java. How do you execute P with JIT-compilation? Which processes (known to operating system) relate to P's execution?