Name	Signature	Student Id Nr	*Points*

581305-6 Computer Organization I, miniexam 1, 14.11.2017 (10p)

Write your answer on this exam paper in the space given. Please notice, that the exam paper is 2-sided.

a) [3 p] Hardware level instruction fetch/execute cycle (instruction cycle), memory references

i. Why do you increment the value of program counter (PC, instruction pointer, IP) by one before the execute phase and not after it?

ii. Assume that current instruction adds 53 to the value in register R1. In which three different ways can the value 53 be referenced in this instruction? Where is the value 53 found in each of these different ways?

iii. How do the memory addresses used by the program differ from those used by the main memory?

How does the hardware know whether a memory address used by the program is good or bad?

How is the main memory address determined?

b) [3 p] Processor execution modes: privileged (supervisor) and user mode.

i. Why do you need the privileged execution mode?

Could you implement the hardware so that it would only have one execution mode?

ii. How does the hardware know that it is in the privileged mode?

How do you get into that mode, and how do you get away from it?

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iii. Give an example on memory area that the program is not allowed to reference in user mode?

Give an example of a privileged instruction that the program is not allowed to use in user mode?

c) [4 p] Interrupts

i. Describe three (3) different types of interrupts (exception, fault). Give an example on each of them.

ii. What happens, if some completely new and unexpected error occurs during instruction execution?

iii. [2 p] Assume that the program tries to use a privileged instruction when the processor is in user mode, and program execution then terminates with an error message.
How do you know in instruction cycle which interrupt handler to invoke?

How is interrupt handler for this error type invoked in the instruction cycle?

What does this interrupt handler do after giving the error message?

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